providing an output data,

said clock signal being a power clock signal having a rising and gradually falling waveform generated by using a charge recycle power source in which power supplied to a load is at least partially collected and returned to said charge recycle power source, and

the following inequality is satisfied:

$|V_{TN}| + |V_{TP}| \geq VDD$

where V_{TN} is a threshold of said n-channel MOSFET transistor, V_{TP} is a threshold of said p-channel MOSFET, and VDD is an output voltage of said charge recycle power source.

4. (Amended) A register circuit according to claim 2, wherein said register circuit includes a combination logic circuit between said pair of D-latch circuits.

5. (Amended) A register circuit according to claim 2, wherein said D-latch circuit comprises a memory element having a first inverter providing an output of the D-latch circuit, a second inverter with an input coupled with an output of said first inverter, and a first transmission gate connecting an output of the second inverter to an input of the first inverter, and a second transmission gate inserted between an input terminal and an input of said first inverter.